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International Journal of Solids and Structures 40 (2003) 7269–7284

INTERNATIONAL JOURNAL OF SOLIDS and STRUCTURES

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Mechanical degradation of microelectronics solder joints under current stressing

Hua Ye, Cemal Basaran *, Douglas C. Hopkins

Electronic Packaging Laboratory, Department of Civil, Structural and Environmental Engineering, State University of New York at Buffalo, 212 Ketter Hall, Buffalo, NY 14260, USA

Received 18 August 2003; received in revised form 18 August 2003

Abstract

Understanding the mechanical degradation of microelectronic solder joints under high electric current stressing is an important step to develop a damage mechanics model in order to predict the reliability of a solder joint under such loading. In this paper, the experiment results for flip chip solder joints under high current stressing are reported. Nano-indentation tests suggest that mechanical property, e.g. Young's modulus, degrades in the localized area where void nucleates during current stressing. The experiments also show that thermomigration due to the thermal gradient within solder joint caused by joule heating is significant during current stressing. A three-dimensional coupled thermal electrical finite element analysis shows the existence of a significant thermal gradient in solder joint during current stressing.

1. Introduction

Electromigration in solder joints under high direct current density is known as a reliability concern for the future high density flip chip packaging and power packaging (Lee et al., 2001; Lee and Tu, 2001; Ye et al., 2002a,b,c, 2003a,b,c). The trend in flip chip and Ball Grid Array (BGA) package to increase I/O count drives the interconnecting solder joints to be smaller in size and, thus, carry higher current density. The current density will increase further as chip voltage decrease and absolute current levels increase. The same trend in current density in interconnecting solder joints is also occurring in flip chip power semiconductors and evolving system-on-package power processors (Liu et al., 1999; Paulasto-Krockel and Hauck, 2001). A physical limit to increasing current density in both microelectronics and power electronics is electromigration. Due to their relatively large size and low current densities electromigration induced failure in solder joints has not been a concern until now. Most research had focused on electromigration of thin metal lines, and little on present day solder interconnects (Brandenburg and Yeh, 1998; Lee et al., 2001; Lee and Tu, 2001).

* Corresponding author. Tel.: +1-716-645-2114x2429; fax: +1-716-645-3733.
E-mail address: cjb@buffalo.edu (C. Basaran).

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doi:10.1016/j.ijsolstr.2003.08.019

Understanding the mechanical degradation of solder joints under high electric current stressing is an important step to develop a damage mechanics model in order to predict the reliability of solder joints. In this paper, the experiment results of flip chip solder joints under high current stressing are reported. Nano-indentation test data suggest that mechanical properties, such as elastic modulus, degrade in the localized area where void nucleates during current stressing. The experiment results also show that thermomigration due to the thermal gradient within the solder joint which is caused by joule heating is significant during current stressing. A three-dimensional coupled thermal–electrical finite element analysis shows the existence of a significant thermal gradient in solder joint during current stressing.

2. Instrumented indentation technique

Instrumented indentation testing (IIT) with a Nano-indenter is a powerful mechanical testing technique that can be used to test extremely small samples. Known as depth-sensing indentation, it collects the indentation load–displacement data precisely on a very small scale. Based on these data, it can measure the material properties such as hardness, Young's modulus, and creep properties on very small scale (micron) specimens. Nano-indentation is very helpful for measuring mechanical properties on solder joints because of the size effect on material properties. By testing specimen the same size as the actual system itself, the size effect is eliminated. Bonda and Noyan (1996) have shown very effectively that at small scale material properties can be significantly different from bulk material. Fig. 1 shows schematic of the equipment for performing instrumented indentation testing, which consists of three basic components: (1) an indenter of specific geometry usually mounted to a rigid column through which the force is transmitted, (2) an actuator for applying the force, (3) a sensor for measuring the indenter displacement.

Continuous Stiffness Measurement technique (CSM), also known as Dynamic Stiffness Measurement, allows for the continuous measurement of elastic stiffness of contact, S, as the indenter is driven in during loading. The measurement is accomplished by superimposing a small force oscillation on the primary loading signal and analyzing the resulting response of the system by means of a frequency-specific amplifier

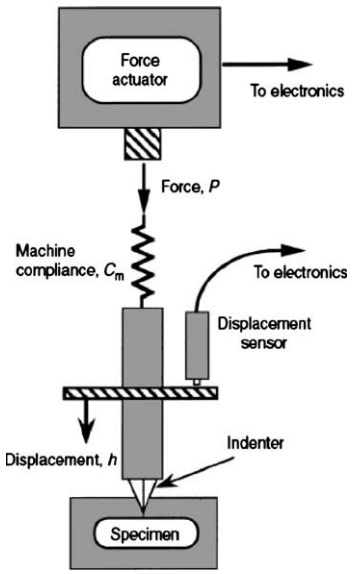

Fig. 1. Schematic representation of the basic components of an IIT system (courtesy to Hay and Pharr (2000)).

(Hay and Pharr, 2000). With a continuous measurement of S, one obtains hardness and Young's modulus as a continuous function of depth of surface penetration. In MTS Nano-indenter XP unit with CSM system, intrinsic or reduced elastic modulus can be determined by the following relation (Hay and Pharr, 2000),

$$E_r = \frac{\sqrt{\pi}}{2\beta}\frac{S}{\sqrt{A}} \tag{1}$$

where S is the elastic stiffness of contact (measured by CSM technique), A is the projected contact area, and β is a constant dependent on the geometry of the indenter. For the MTS Nano-indenter XP which uses a Berkovich tip, $\beta = 1.012$. Berkovich indenter tip has a three-sided pyramid shape. It has a centerline-to-face angle α of 65.3°, projected area of $24.56d^2$ (d is the indentation depth), and volume depth relation of $8.1873d^3$ Fig. 2 shows a picture of the impression on an actual solder joint after indentation with Berkovich indenter.

The reduced modulus E_r is used to account for the fact that elastic displacement occurs in both the indenter and sample. The Young's modulus of the tested material, E, is calculated by:

$$\frac{1}{E_r} = \frac{1-v^2}{E} + \frac{1-v_i^2}{E_i} \tag{2}$$

where v is the Poisson's ratio for the tested material, and E_i and v_i are the elastic modulus and Poisson's ratio of the indenter respectively. For diamond indenter, the elastic constants $E_i = 1141$ GPa and $v_i = 0.07$ are often used (Simmons and Wang, 1971; Oliver and Pharr, 1992).

For the purpose of calculating E, the projected contact area, A, must be accurately obtained. The projected contact area is calculated by evaluating an empirically determined area as a function of the contact depth, h_c,

$$A = f(h_c) \tag{3}$$

This area function, also known as the shape function or tip function, relates the cross-sectional area of the indenter to the distance from its tip. Contact depth, h_c, is the depth over which the test material makes contact with the indenter, and is generally different from the total penetration depth, h, by

$$h_c = h - \varepsilon P/S \tag{4}$$

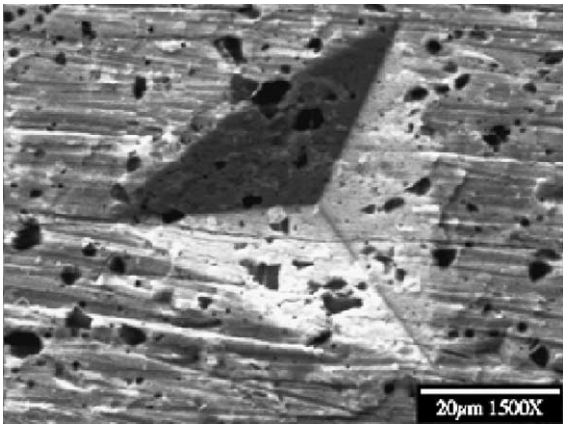

Fig. 2. Indentation on a solder joint with a Berkovich indenter.

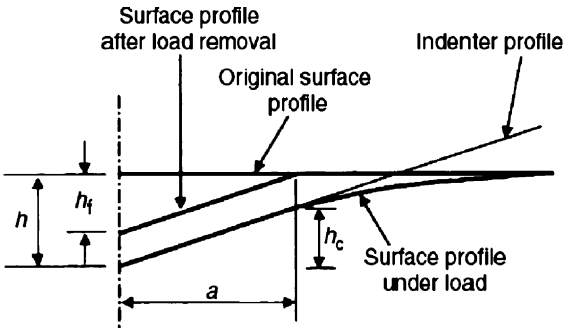

Fig. 3. Schematic representation of a section through an axisymmetric indentation showing various quantities used in analysis (after Hay and Pharr (2000)).

where ε is a constant, which depends on indenter geometry. The empirical value of ε for Berkovich indenter is 0.75 (Oliver and Pharr, 1992). P is the load applied to the test surface. This relationship is based on elastic contact theory, but it works well even when contact causes significant plastic deformation (Oliver and Pharr, 1992). Fig. 3 shows a schematic of the indentation process for an axisymmetric indenter, where h_c and h are schematically shown.

Once the projected contact area (A) and contact stiffness (S) are known, the Young's modulus can be calculated by Eq. (2). In the experiment, indentation tests were conducted on several locations on each solder joint in order to get the distribution of Young's modulus over the solder joint.

3. Experimental set-up

The test flip chip modules were produced in an industrial lab to attain consistent interconnects representative of high volume commercial manufacturing. The test module has a dummy silicon die with only aluminum (Al) conductor trace on it. The silicon die is attached on a FR4 printed circuit board (PCB) through eutectic Pb37/Sn63 solder joints. The copper plates on the PCB provide the wetting surface and electric connection to the solder joints. The under bump metallization (UBM) on silicon die side is electroless Ni. The voids between the solder joints are filled with underfill between the silicon die and PCB substrate. The thickness of the Al trace is about 1 μm and the width is about 150 μm. The diameter of the solder joint is around 150 μm and the height is about 100 μm. The test module was cross-sectioned and finely polished towards the center of the solder joints before current stressing. On each module, two solder joints were tested. The solder joints on each test module is named in such a way that current always flows from copper trace through solder A into the Al trace on silicon die and then flow through solder B out to another copper trace. Fig. 4 shows the schematic cross-section of the test module and the direction of current flow in the experiments.

Three test modules were subjected to current stressing at 0.9–1 A, which lead to a current density near 1×10^4 A/cm^2 in the cross-sectioned solder joint. The exact current density value in the solder joint may vary since it is difficult to polish to the exact center of solder joint. An example of sectioned and polished solder joint is shown in Fig. 5. The solder joint in Fig. 5 does not show an aspect ratio of 150 μm in width and 100 μm in height. This is because that the solder joint was not polished into its center. Fig. 5(a) shows no UBM on the Si die side, indicating that the solder joint was not polished into the region of UBM. Fig. 5(b)–(e) show a small area of UBM on the Si die side after re-polishing following 37.5 h of current stressing. We took this into consideration when we estimate the current density. Nano-indentations were performed on each solder joint before current stressing to get the initial mechanical properties. The test modules were then

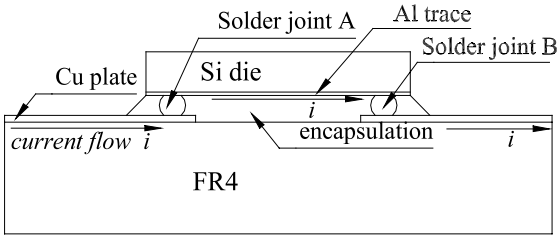

Fig. 4. Schematic cross-section of the test module.

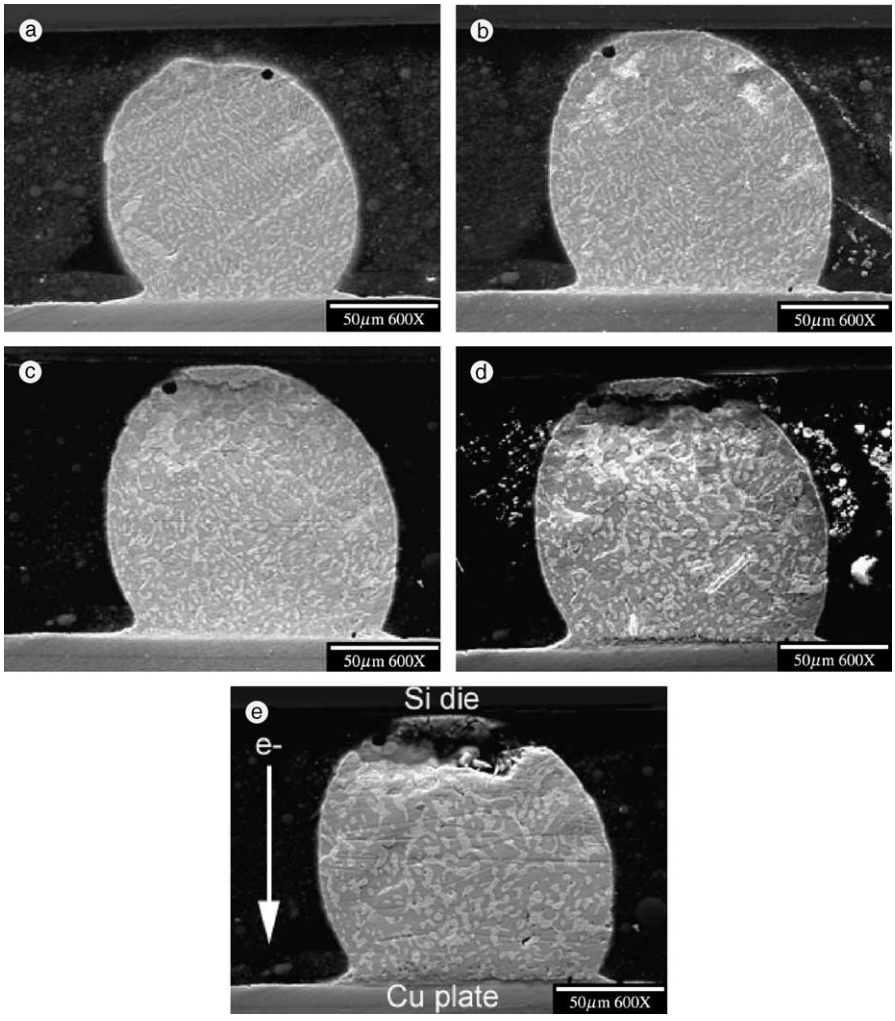

Fig. 5. Secondary SEM of solder joint A on Module #1: (a) initial, (b) 37.5 h (re-polished), (c) 60.5 h, (d) 129.5 h, (e) 178 h.

subjected to current stressing. During the course of current stressing, the test modules were taken off the circuit for Scanning Electron Microscopy (SEM) analysis and nano-indentation testing. Fig. 5(a)–(e) and

6(a)–(e) show the SEM images of solder joints A and B in Module #1 during current stressing, respectively. Both solder joints were subjected to nano-indentation testing after 37.5 h of current stressing and then re-polished for further current stressing. After 129.5 h of current stressing, severe void nucleation is observed on solder A near Si die side (which is cathode) as expected since the direction of electromigration is from cathode to anode. Hillock is observed near Cu plate side on solder A. Void nucleation is also observed on solder B near Si die side which is anode side. Although the void nucleation on solder B near Si die side is less severe compare to that of solder A, electromigration alone cannot explain this observation. If electromigration were the only driving process in microstructure evolution of solder B, void nucleation should be expected to occur near cathode side, e.g. Cu plate side, which was not the case. Similar observations were observed on other two test modules. This observation indicates that there has to be another competing process besides electromigration during current stressing.

It is suspected that thermomigration is responsible for the response observed in solder joint B. Since the Al trace on the Si die side contributes to the most of the electric resistance in the test module, majority of

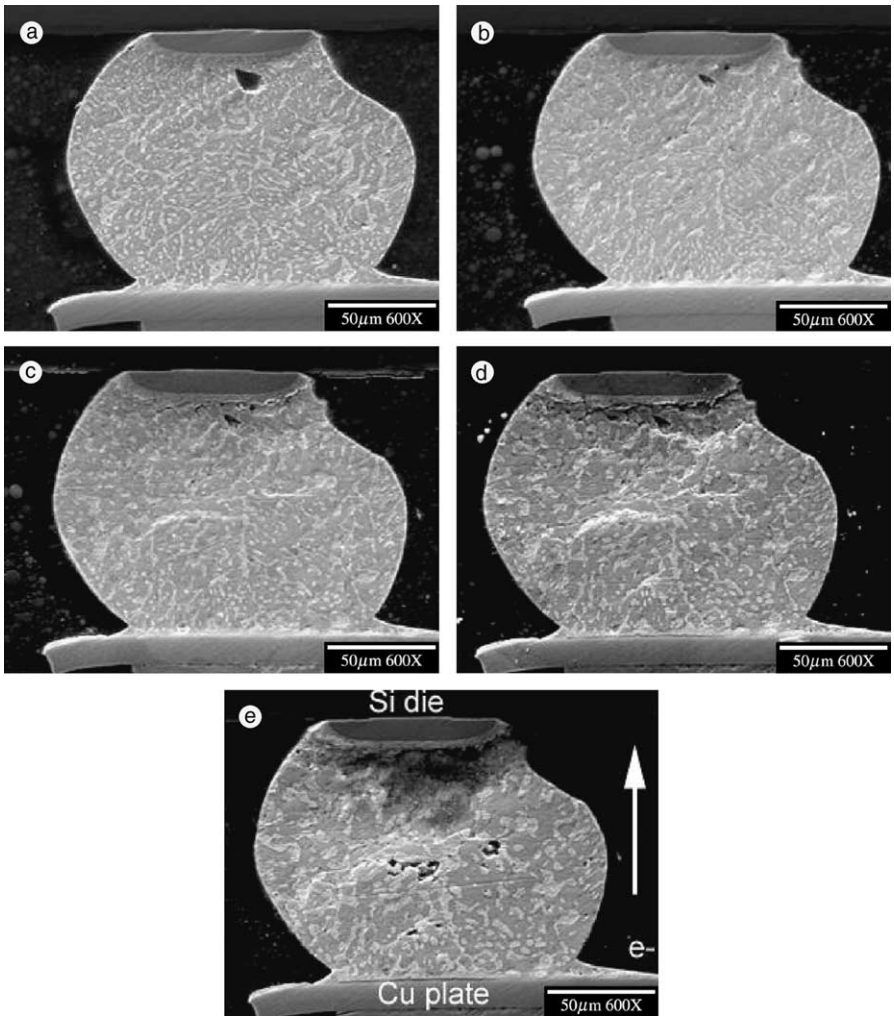

Fig. 6. Secondary SEM of solder joint B on Module #1: (a) initial, (b) 37.5 h (re-polished), (c) 60.5 h, (d) 129.5 h, (e) 178 h.

the joule heating is generated in Al, which makes the silicon die very hot. During the experiments, the temperature on top of the silicon die of different test modules measured by a thermal coupled ranged from 70 to 150 °C. Thus it is reasonable to assume that there is a thermal gradient in the solder joint during current stressing. This assumption is verified by a three-dimensional coupled thermal–electrical finite element (FE) simulation of the actual test module, which will be discussed in the following section. Thermomigration would occur in the solder joint in the presence of a thermal gradient. Roush and Jaspal (1982) observed the thermomigration of Pb/In solder alloy at a thermal gradient of 1200 °C/cm and reported that both In and Pb move in the direction of the thermal gradient. Van Gurp et al. (1985) reported fast thermomigration in In and In alloy films and found material is transported from hot to cold areas. Thermomigration in pure Pb has been observed by Johns and Blackburn (1975) over the temperature range of 322–202 °C. They reported that in all circumstances flow of material was from hot to cold. In our experiments, mass diffusion in eutectic Pb/Sn solder B is from hot side (Si die side) to cold side (Cu plate side), which agrees with above mentioned reports. Thermomigration may assist electromigration if the hot side coincides with cathode side as in solder A or it may counter electromigration if hot side coincides with anode side as in solder B. If thermomigration outperforms electromigration in the overall diffusion process, voids nucleation would occur near anode side as in the case of solder B as shown in Fig. 6. Thermomigration can also explain the observation that more severe voids nucleation near Si die side in solder A than in solder B. This observation suggests that thermomigration may not be omitted in the electromigration analysis of flip chip solder joint when joule heating from Si die is not negligible. Thermomigration is a complex mass motion process in a thermal gradient region. The driving force of thermomigration can be divided into two categories, intrinsic and thermal. The intrinsic part includes the energy transported by the moving atoms; the thermal part includes the interactions with the usual heat carriers in the lattice, electrons and photons.

Assuming that the metal atoms migrate via a vacancy diffusion mechanism, the flux of metal atoms is equal and opposite to the flux of vacancies. Following Kircheim (1992) the flux of vacancy in a metal due to electron wind force is

$$\vec{J}_{\mathrm{em}} = -\frac{DC}{kT} Z^* e \vec{\nabla} \Psi \tag{5}$$

where D is vacancy diffusivity, C is vacancy concentration, k is Boltzman's constant, Z^* is vacancy effective charge number, e is electron charge, Ψ is electric potential field. The flux of vacancy due to hydrostatic stress gradient given by Kircheim (1992) is

$$\vec{J}_{\sigma} = -\frac{DC}{kT} f \Omega \vec{\nabla} \sigma \tag{6}$$

where f is vacancy relaxation ratio (the ratio between the relaxation volume of a vacancy and the volume of an atom), Ω is atomic volume. If there exists a thermal gradient in the metal, the flux due to thermomigration by Hungtington (1972) is

$$\vec{J}_{\mathrm{th}} = -\frac{DC}{kT^2} Q^* \vec{\nabla} T \tag{7}$$

where Q^* is heat of transport, the isothermal heat transmitted by the moving atom in the act of jumping, less its intrinsic enthalpy. By combining all the above flux components plus the flux generated by the vacancy concentration gradient, the total vacancy flux in a metal under current stressing is thus

$$\vec{J}_{\mathrm{tot}} = -D\left(\vec{\nabla} C + \frac{C}{kT} Z^* e \vec{\nabla} \Psi + \frac{C}{kT^2} Q^* \vec{\nabla} T + \frac{C}{kT} f \Omega \vec{\nabla} \sigma\right) \tag{8}$$

This diffusion equation can be used to describe the diffusion behavior of solder alloy under current stressing without assuming a uniform temperature field. It shows that if the thermal gradient is not negligible, thermal migration may assist or counter electromigration diffusion depending on the directions of electric gradient and thermal gradient. The vacancy continuity equation is thus (Kircheim, 1992),

$$\frac{\partial C}{\partial t} = -\nabla \cdot \vec{J}_{\text{tot}} + G \tag{9}$$

where G is vacancy generation/annihilation rate.

4. Nano-indentation experiments

Since the ultimate goal of this research project is to develop a damage mechanics model for solder joints under high current density stressing, it is important to investigate the mechanical property degradation of solder alloy during this process. Nano-indentation tests were performed on the solder joint before current stressing to obtain the initial mechanical properties. Then the solder joint was re-polished and subjected to current stressing. After certain number of hours of current stressing, the module was taken off the circuit and the solder joints were re-polished again. Nano-indentation was performed to get the change in mechanical properties. This scheme is possible since the indentation depth is controlled to be 2 μm and thus only a very thin layer (several microns) needs to be polished away after indentation. After the first set of indentations, the residual stress within the solder joint, due to the plastic deformation caused by indentations, may alter its mechanical properties. However, the indentation depth was only 2 μm, hence the plastic deformation only occurs in the region very near to the surface. When the specimen was re-polished, a layer of several microns was polished away; therefore, the residual stress from the first set of indentation would not affect the results from the second set of indentations.

In continuum damage mechanics, the damage variable, D, represents a measure of material deterioration during various physical phenomena. For undamaged material, $D = 0$; for damaged material, $0 < D < 1$. An effective way to measure damage is based on the influence of damage on elasticity, $\widetilde{E} = E(1 - D)$, where $\widetilde{E}$ is effective Young's modulus of the damaged material and E is the Young's modulus of undamaged material. Thus, the value of damage may be derived from measurements of $\widetilde{E}$ (Lemaitre, 1996)

$$D = 1 - \frac{\widetilde{E}}{E} \tag{10}$$

Basaran and Tang (in press) have experimentally shown that this is the most stable criterion to quantify degradation of ductile solder alloys. From physics perspective, elastic modulus is directly related to the atomic bond. Damage decreases the atomic bonds, hence reduces the elasticity. When void nucleates in the solder joint during current stressing, the material is viewed as damaged at the mesoscale and the value of damage is proportional to the density of microvoids. Thus we expect the measured effective Young's modulus to decrease in the area of void nucleation. Since the void nucleation is localized as described earlier, the damage or the decrease in effective Young's modulus is also expected be localized. With the ability of nano-indentation to measure the Young's modulus in an extremely small area, the localized evolution of modulus on the solder joint during current stressing can be captured. The indentation method used in the experiment is ''MTS XP CSM Standard Hardness, Modulus, and Tip Calibration'', where contact stiffness and thus, modulus are continuously calculated by dynamic measurement technique. Loading is controlled such that the indenter tip penetration velocity divided by penetrating depth (defined as strain rate target) was held constant at 0.05/s. The maximum indentation depth was set to be 2000 nm in the tests. Fig. 7 shows the load vs. displacement into surface curve for an actual indentation on one solder joint.

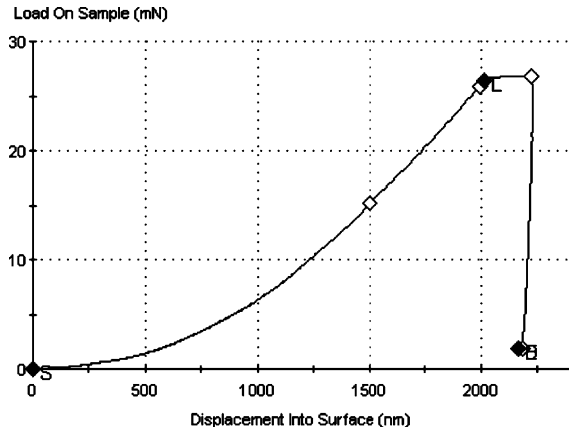

Fig. 7. Load vs. displacement into surface for an indentation.

Fig. 8 shows the modulus vs. displacement into surface curve for that indentation, where the modulus was calculated based on the aforementioned theory. Since the contact stiffness, S, was continuously measured, the modulus is presented as a continuous curve. Although the modulus is continuously measured throughout the penetration depth from 0 to 2000 nm, the reported Young's modulus value is averaged over the penetration depth from 1500 to 2000 nm in order to eliminate any size effect or inaccuracy at small indentation depth. Throughout our tests, the measured modulus for majority of the solder joints follows a similar tendency: the modulus at small indentation depth is much greater than that at larger depth and decreases with indentation depth until it reaches a relatively stable value as shown in Fig. 8.

This observation agrees well with results of many nano-indentation size effect experiments, which has been an active research topic for many years and strain gradient theory is the most widely used theory to explain this phenomenon (Nix and Gao, 1998; Gao and Fan, 2002; Gerberich et al., 2002; Ning et al., 2003; Elmustafa and Stone, 2003). However, size effect is not the focus of this research; therefore, average modulus from a depth of 1500 to 2000 nm is chosen for the purpose of comparison between different stressing times.

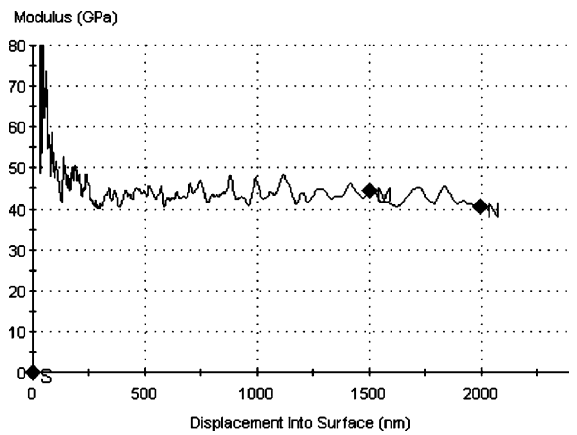

Fig. 8. Modulus vs. displacement into surface for an indentation.

In order to pinpoint the distribution of effective Young's modulus, nano-indentations were performed on different locations on each solder joint as shown in Fig. 9(a) in the experiment. In order to illustrate the distribution of Young's modulus within a solder joint, a non-dimensional coordinate system is employed. In this coordinate system, 0 denotes the interface between copper and solder and 1 denotes the interface between solder and silicon from Cu–solder interface to solder–silicon interface as shown in Fig. 9(b). Nano-indentation tests were performed on each solder joint before and after certain time of current stressing to explore the evolution of modulus degradation during stressing.

Figs. 10–15 show the distribution of measured elastic modulus from nano-indentation for each solder joint on the dimensionless coordinate before and after current stressing. Since several indentations were conducted at a single coordinate position, both the measured values and their average are shown in these figures. As shown in these figures, the decrease of Young's modulus is clear for each solder joint after current stressing. In all cases, the maximum drop in modulus is always near the solder–silicon interface no matter what the direction of electron flow is, which agrees with SEM observation that void nucleation is also always in this region. In the region near the Cu–solder interface, there is no drop of modulus or the drop in modulus is considerably smaller than that in region near solder–silicon interface. This observation also confirms that thermomigration was actually taking the leading role during the current stressing. It

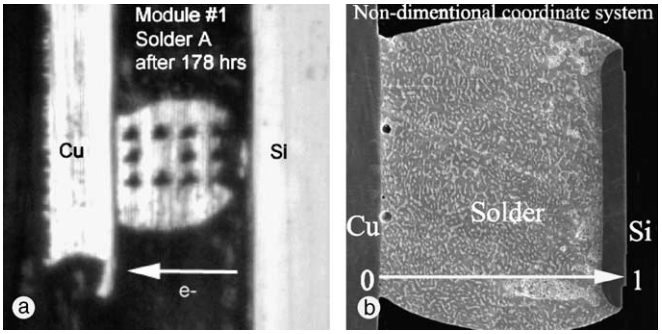

Fig. 9. (a) Distributed nano-indentations on solder joint. (b) Schematic of the non-dimensional coordinate.

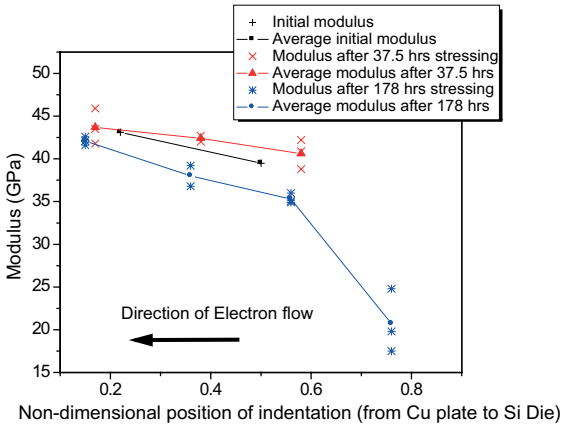

Fig. 10. Evolution of modulus distribution on the non-dimensional coordinate system during current stressing for solder A, Module #1.

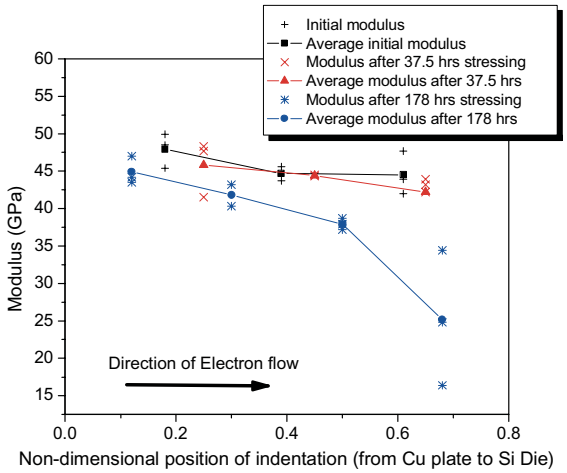

Fig. 11. Evolution of modulus distribution on the non-dimensional coordinate system during current stressing for solder B, Module #1.

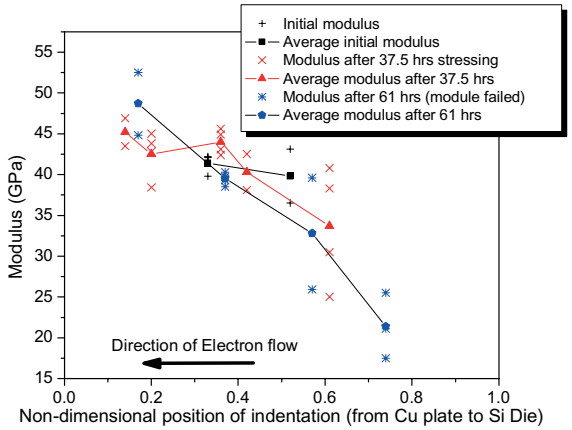

Fig. 12. Evolution of modulus distribution on the non-dimensional coordinate system during current stressing for solder A, Module #2.

indicates that the damage in solder joint during current stressing is very much localized and only in the regions of void nucleation would the mechanical damage accumulate. Apart from the general trend that measured modulus is always higher near solder–Cu plate interface, and lower near solder–Si die interface, the modulus distribution of solder joint B after 865 h of stressing in Module #3 is rather zigzag as shown in Fig. 15. This anomaly could be due to non-homogeneous diffusion within this solder joint during current stressing.

Table 1 shows the maximum measured damage as defined in Eq. (10) in each solder joint after certain hours of current stressing. The effective modulus used in calculation is taken from the average measured modulus at the positions nearest to the solder–Si interface; the undamaged modulus is taken as the total average modulus from the measurements of the virgin solder joint. The module eventually failed at the end of the testing when the damaged solder joint cannot sustain the applied mechanical and thermal loading.

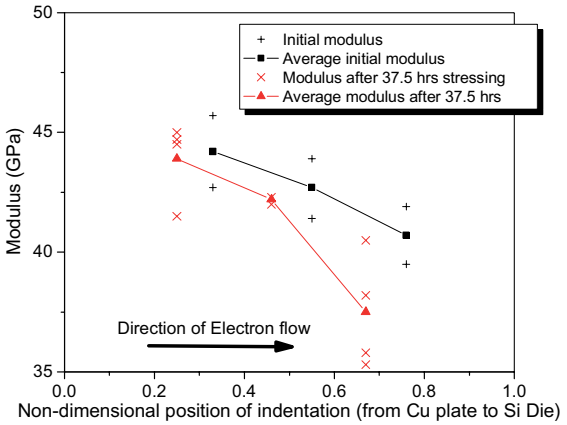

Fig. 13. Evolution of modulus distribution on the non-dimensional coordinate system during current stressing for solder B, Module #2.

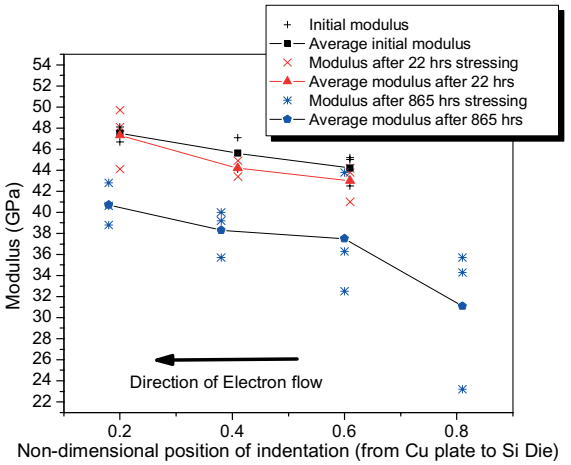

Fig. 14. Evolution of modulus distribution on the non-dimensional coordinate system during current stressing for solder A, Module #3.

Module #1, #2, and #3 failed after a total of 256, 61, and 960 h of current stressing, respectively. Table 1 clearly shows that absolute current level is not a prominent factor for mechanical degradation of solder joint, since with current level about the same, the solder joints in Module #3 still had much less D_{max} even after much longer time of stressing. Whereas, the current density and stressing temperature seems to control the degradation of solder joint during current stressing. For example, solder joints in Module #2, which had the highest current density and stressing temperature, had the fastest mechanical degradation. This is because that higher current density leads to faster electromigration; higher stressing temperature leads to greater thermomigration since higher temperature on the silicon die indicates higher temperature gradient within the solder joint as illustrated by the coupled thermal–electrical FEM simulation. Higher temperature also leads to greater solder diffusivity, which will accelerate both thermomigration and electromigration.

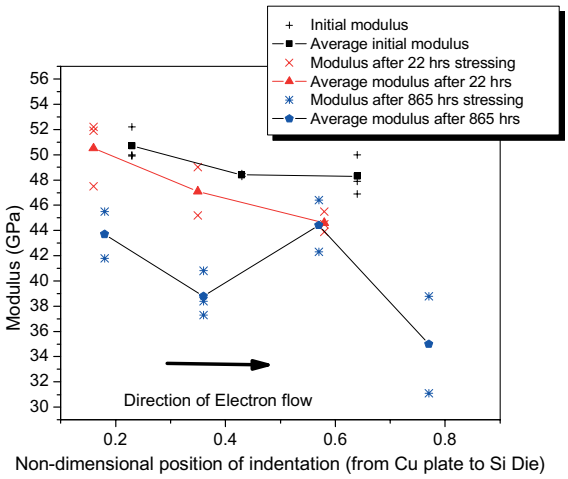

Fig. 15. Evolution of modulus distribution on the non-dimensional coordinate system during current stressing for solder B, Module #3.

Table 1
Maximum measured damage in the solder joints

Module #	Current level (A)	Stressing temperature (°C)	Stressing time (h)	Solder	Current density (10^4 A/cm^2)	D_{max}
1	1	120	178	A	0.72	0.51
				B	0.73	0.45
2	1	150	61	A	0.96	0.48
				B	1.0	n/a
3	0.9	100	865	A	0.62	0.32
				B	0.61	0.29

5. Coupled thermal–electrical FEM simulation

A three-dimensional coupled thermal electrical FE simulation of the flip chip test module is conducted to determine the temperature distribution within the solder joint. Since during the experiment the test module was cross-sectioned through the center of the solder joint, only cross-sectioned module is modeled in the simulation. In the FE model, the thickness of the Al trace is 1 μm and the width is 150 μm. The solder joint has a diameter of 150 μm and a height of 100 μm. Due to the symmetric geometric structure of the module, only half of the module is modeled. Joule heating due to the electric current is the only heat source in the model. The thermal boundary condition is that the temperature on the far end surface of the PCB is fixed at room temperature, 23 °C. The thermal radiation is considered for all external surfaces of the module and an emissivity of 0.7 is assumed. The electric potential is fixed to be 0 at one end of the Al trace and a concentrated current load is applied at the other end of Cu plate. The material properties used in the simulation are taken from Pech et al.'s (1998) as shown in Table 2. The temperature distribution for the case of 1 A current loading is shown in Fig. 16. The Al trace and Si die has the highest temperature 150 °C, which is close to the thermal couple measured temperature in the test. The temperature distribution on the solder joint alone is shown in Fig. 17. Fig. 18 shows temperature gradient through a vertical line across the solder joint. The temperature on the Si–solder interface is 15 °C higher than that on the solder–Cu interface within

Table 2
Material properties (Pecht et al., 1998)

	Thermal conductivity (W/cm °C)	Electric conductivity (Ω^{-1} cm^{-1})	Density (g/cm^3)	Thermal capacity (J/g °C)
Al	2.37	3.1×10^5	2.7	0.894
Cu	4.03	4.89×10^5	9	0.385
FR4	0.015	5×10^{-14}	2.54	1.0
Si	1.5	1.56×10^{-5}	2.3	0.712
Solder	0.506	6.9×10^4	8.48	0.134
Underfill	0.03	1×10^{-14}	1.15	1.6

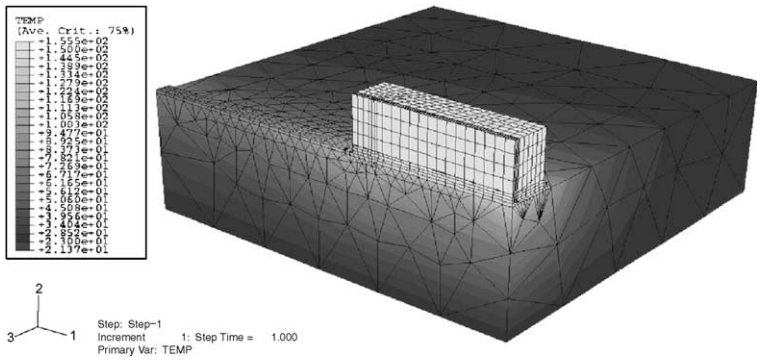

Fig. 16. Temperature distribution within the module for 1 A current.

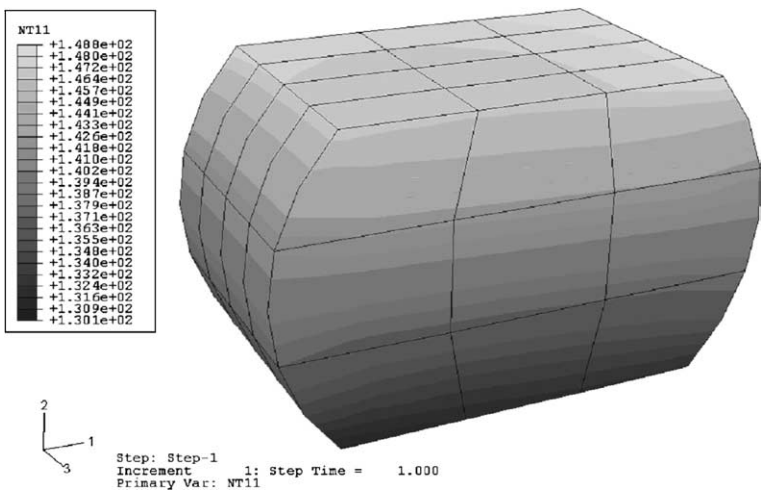

Fig. 17. Temperature distributions within the solder joint for 1 A current.

a distance of only 100 μm. Therefore, a thermal gradient of 1500 °C/cm is predicted in the simulation, which exceeds the thermal gradient reported by Roush and Jaspal (1982), 1200 °C/cm, for his observation of thermomigration.

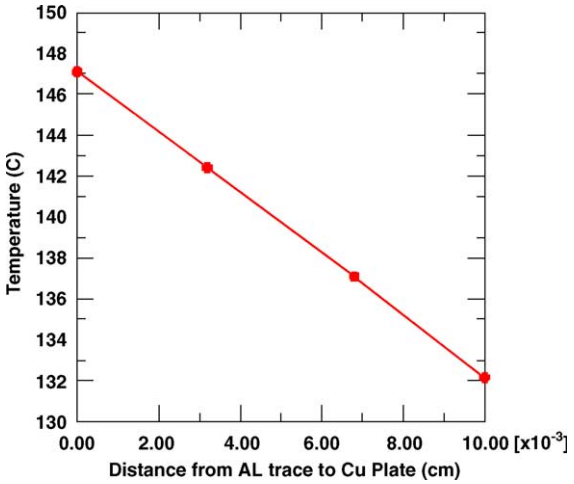

Fig. 18. Temperature distribution along the vertical line across the solder.

6. Conclusions

In this paper, the experimental results for flip chip solder joints under high current density stressing are reported. Nano-indentation tests show that elastic modulus of solder joint degrades during high current density stressing. The decrease of modulus (or damage) is localized in the area where void nucleates during current stressing. The experiments also show that thermomigration due to the thermal gradient within solder joint caused by joule heating is significant during current stressing and may dominate the migration (void nucleation and coalescence) process. A three-dimensional coupled thermal electrical finite element analysis shows that the existence of thermal gradient in solder joint during current stressing is significant.

Acknowledgements

This project is sponsored by the U.S. Navy, Office of Naval Research, Advanced Electrical Power Systems program under Mr. Terry Ericsen and by International Microelectronics and Packaging Society (IMAPS). We gratefully acknowledge all the help we received from Dr. Darrel Frear and Dr. Jong-Kai Lin of Motorola Inc., Tempe, AZ who provided all the flip chip test vehicles.

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